PMm2 ASIC: PARISROC

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Abstract

PARISROC is a complete read out chip in AMS SiGe 0.35µm technology for photomultipliers array. It is made to allow triggerless acquisition for next generation neutrino experiments. The ASIC integrates 16 independent channels with variable gain and provides charge and time measurement with a 12-bit ADC and a 24-bits Counter.

I. INTRODUCTION

The PMm2 project [1] proposes an innovative electronics for array of photo-detectors used in High Energy Physics and Astroparticle. The goal is to develop a macro pixel made of 16 small photomultiplier tubes connected to an autonomous front-end electronics, as shown in Figure1, in order to segment very large surface of photo-detection.

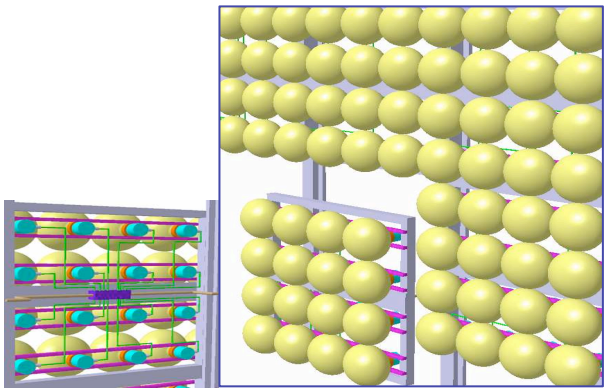


Figure 1: 16 PMT module with central ASIC

This R&D [2] involves three French laboratories (LAL Orsay, LAPP Annecy, IPN Orsay) and PHOTONIS company, the French photomultiplier tube maker as shown in figure 2. It is funded for three years by the French National Agency for Research (ANR) under the reference ANR-06-BLAN-0186.

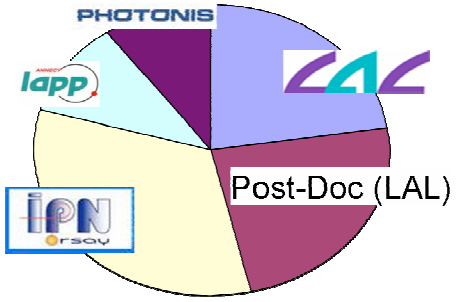


Figure 2: PMm2 group

The micro-electronics group (OMEGA) from the LAL at Orsay is in charge of the front-end electronics and develops an ASIC called PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) described below.

II. ASIC ARCHITECTURE

A. Requirements

The Electronics must be autonomous, triggerless and with 16 independent channels. It must provide charge and time measurements. The charge measurement has to be efficient for 1 photo-electron and with a good linearity on a dynamic range up to 300 photo-electrons. The time measurement is done in two steps: a coarse measure with a 24 bit counter at 10MHz and a fine measure on a 100 ns ramp to achieve a resolution of 1ns. Because of the common high voltage supply, the preamplifier gain must be adjustable channel by channel in order to compensate the photomultiplier tube gain variation. Output data are serialized to be sent by only one communication wire.

B. Global architecture

The global architecture of the ASIC is shown in figure 3. It is composed of 16 analogue channels managed by a common digital part.

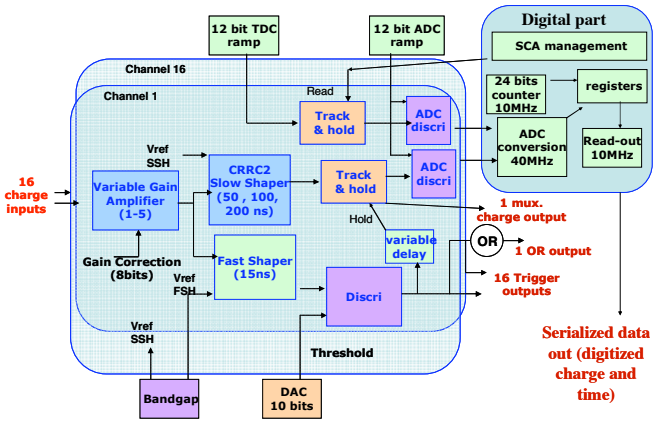


Figure 3: PARISROC global schematic

A bandgap bloc provides the common voltage references for fast and slow shapers. The threshold of the discriminators is common for the sixteen channels and given by a 10 bit DAC. The ramps for ADC and TDC are common for all the channels.

C. One channel detail

The detail of one analogue channel is given in figure 4. Each channel is composed by a low noise preamplifier with

variable and adjustable gain. The variable gain is common for all channels and can change from 8 to 1 on 4 bits. The gain is also adjustable channel by channel by a factor 4 on 8 bits.

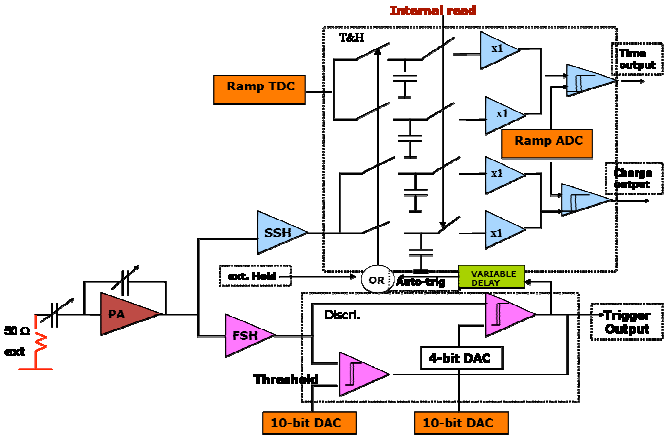


Figure 4: One channel schematic

The preamplifier is followed by a slow channel for the charge measurement in parallel with a fast channel for the trigger output. The slow channel is made by a slow shaper followed by an analogue memory with depth of 2 to provide a linear charge measurement up to 50pC; this charge is converted by a 12 bit Wilkinson ADC. The fast channel is composed of a fast shaper (15ns) followed by 2 low offset discriminators to auto-trig down to 10fC. The thresholds are loaded by 2 internal 10-bit DACs common for the 16 channels plus a 4bit DAC per channel for one discriminator. The 2 discriminator outputs are multiplexed to provide only 16 trigger outputs.

The fine time measurement is made by an analogue memory with depth of 2 which sample a 12 bit ramp as the same time of the charge. This time is then converted by a 12 bit Wilkinson ADC.

D. Digital part

On overview of the digital part is given in figure 5. The digital bloc manages the track and hold system like a FIFO and starts and stops all the counters [3]. All the data are serialized to be sent out.

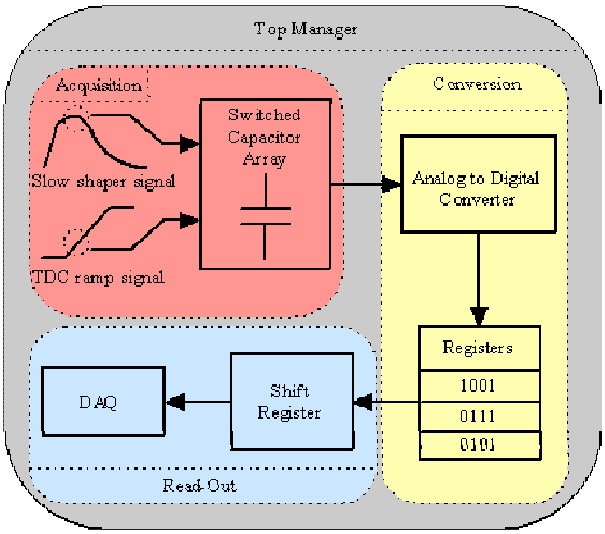


Figure 5: Digital part overview

There are two clocks: one at 40 MHz for the analogue to digital conversion and for the track and hold management, the second at 10MHz for timestamp and readout.

The readout format is 52 bits: 4bits for channel number + 24 bits for timestamp + 12 bits for charge conversion + 12 bits for fine time conversion. The readout is selective: only the hit channels are read; so the maximum readout time will be 100µs if all channels are hit.

E. PARISROC layout

Figure 6 presents the PARISROC layout. The circuit has been designed in AMS SiGe 0.35µm technology [4]. The die has a surface of 17 mm^2 (5mm X 3.4mm) and will be package in CQFP160 case.

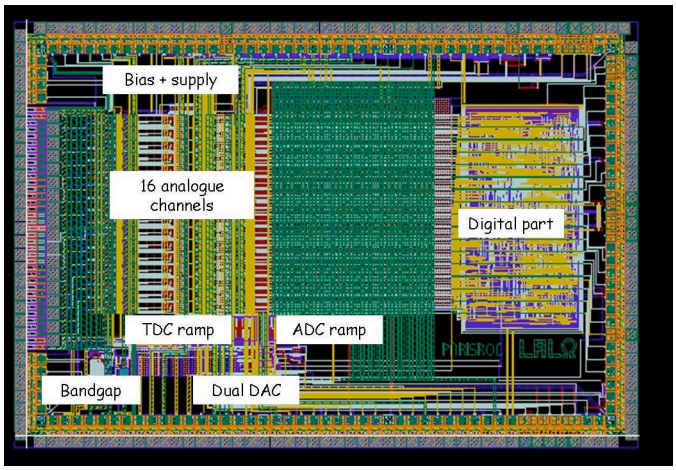


Figure 6: PARISROC layout

PARISROC was sent in foundry on June and the dies are expected for the end of September 2008.

III. Analogue Channel Simulations

A. Preamplifier

1) Input signal

For all the simulations, except for the photomultiplier gain adjustment, we use a triangle as input signal to simulate the photomultiplier signal. It is a 4.5ns rise and fall time with a 1ns duration current signal as shown in figure 7. This current signal is sent on an external resistor (50 Ohms) and varies from 0 to 10mA in order to simulate a PMT charge from 0 to 50pC which represents 0 to 300 photo-electrons when the PM gain is 10^6

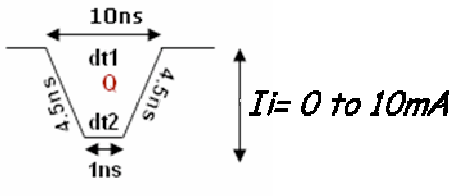


Figure 7: Input signal used for simulation

2) Preamplifier response

The preamplifier gain is given by the ratio between the input capacitance (Cin) and the feedback capacitance (Cf). This gain can vary from 8 to 1 by changing Cin on 4 bits for the sixteen channels together.

The figure 8 gives the preamplifier response at gain 4 for an input charge from 0 to 50pC

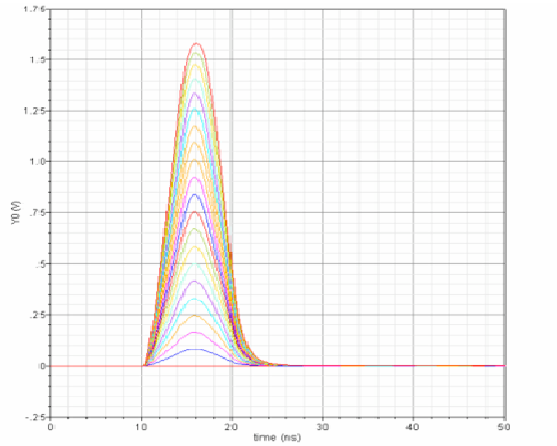
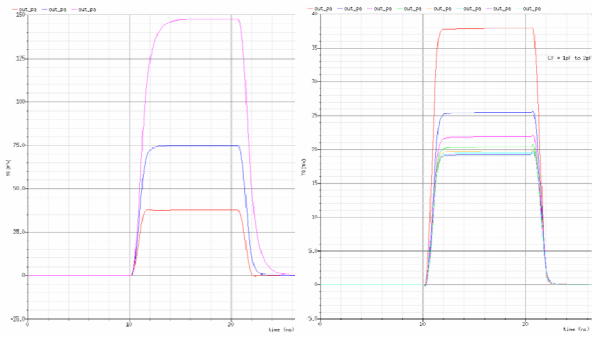


Figure 8: preamplifier response at gain 4 with input charge from 0 to 300 photo-electrons

3) Photomultiplier gain adjustment

On the preamplifier the feedback capacitance (Cf) value could be changed to adjust the photomultiplier plus preamplifier gain channel by channel. The typical value of Cf is 0.5pF and can be changed by a factor four on 8 bits (from 125fF to 2pF by step of 17fF). The figure 9 shows the preamplifier output for the same input charge (a square pulse with 1ns rise and fall time and 9ns duration) when the feedback capacitance varies.



(a) (b)

Figure 9: Preamplifier output for various Cf (a: from 1pF to 2 pF, b : from 0.25pF to 1pF)

B. Slow shaper

1) Response at 1 photo-electron

The shaping time constant can be chosen between 50ns, 100ns or 200ns but it is common for all channels. The slow shaper response at one photo-electron for the various time constant is shown in figure 10 and the main characteristics (gain, peaking time, noise and signal over noise) of these signals are listed in Table 1.

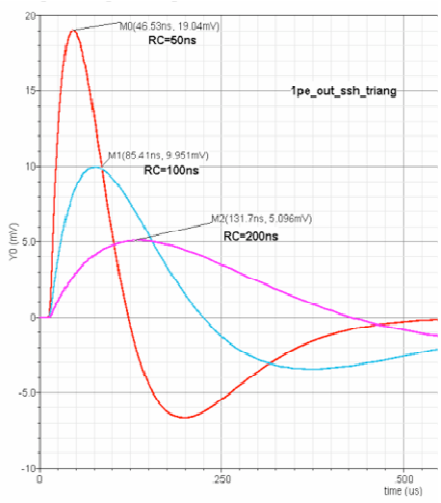


Figure 10: Slow shaper response at 1 p.e. for various shaping time

Table 1: Slow shaper specifications for various time constant

Time constant	Vout	RMS noise	S/N
50ns	19mV @ Tp=37ns	1.6mV	11
100ns	10mV @ Tp=75ns	1.2mV	8
200ns	5mV @ Tp= 122ns	950µV	5

2) Linearity

Figure 11 gives the simulation of the linearity for preamplifier gain 8 and 4. For the preamplifier gain 4, the non-linearity is very good (less than 0.5%) for an input charge until 330 photo-electrons. Of course when the gain doubles the input dynamic range is divided by two for the same non-linearity.

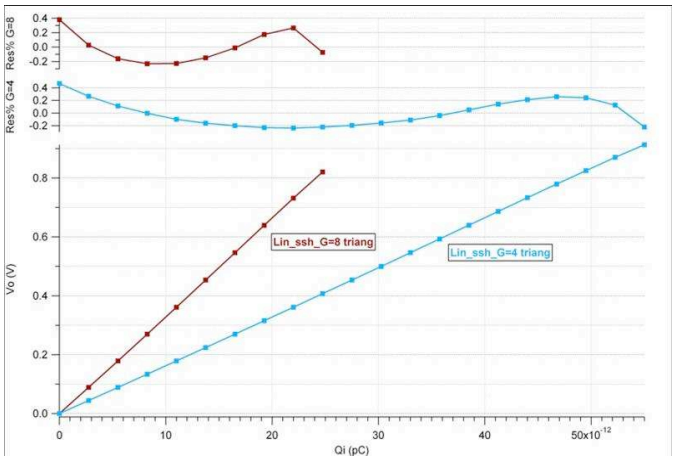


Figure 11: Slow shaper linearity and residuals for gains 4 and 8

3) Slow shaper response

The slow shaper is a CRRC2 with variable time constant. The figure 12 shows the slow shaper response with an input charge from 0 to 2pC. The gain of the preamplifier is 4 and the time constant of the shaper is 200ns.

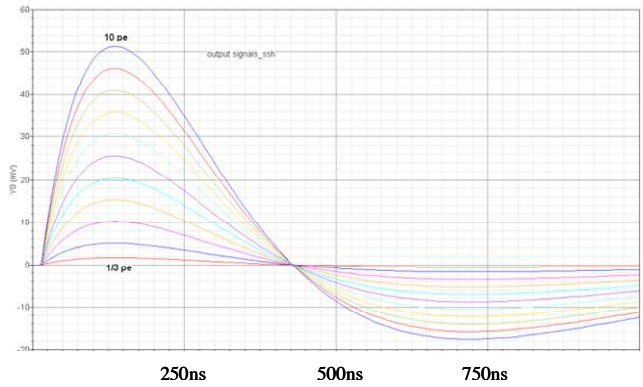


Figure 12: Slow shaper response for input from 1/3 to 10p.e.

C. *Fast shaper*

The fast shaper is a CRRC with a time constant of 15ns and with high gain to send high signal to discriminator. The goal is to trigger easily on the third of photo-electron. The figure 13 shows the fast shaper response for an input charge from 0 to 2pC.

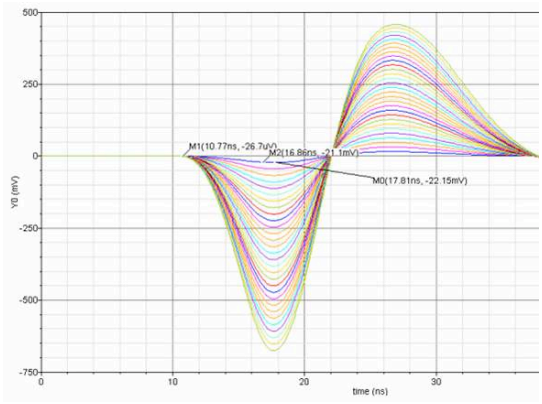


Figure 13: Fast shaper response for input from 0 to 10 p.e

The fast shaper response at one photo-electron is a signal of 65mV at a peaking time of 7ns. The RMS noise is around 2.3mV which gives a signal over noise ratio of 28.

D. *Discriminator*

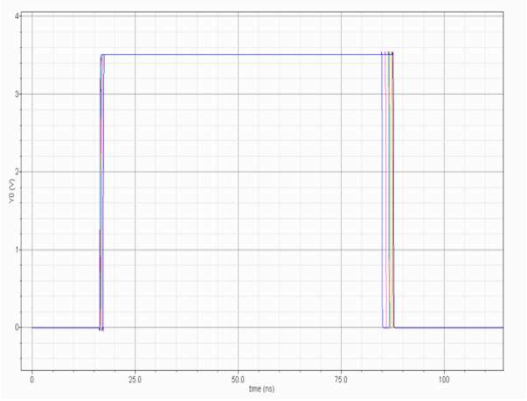


Figure 14: Discriminator output for an input charge from 0 to 10 p.e. with a threshold at 1/3 p.e

The discriminator is only a simple low offset comparator. The threshold is common on the 16 channels and provided by a 10 bit DAC. The threshold can be set at one third of the photo-electron. The output duration depends on the input signal amplitude as shown in figure 14. Figure 15 is an enlargement of the discriminator rise time in order to see the time walk of around 4 ns.

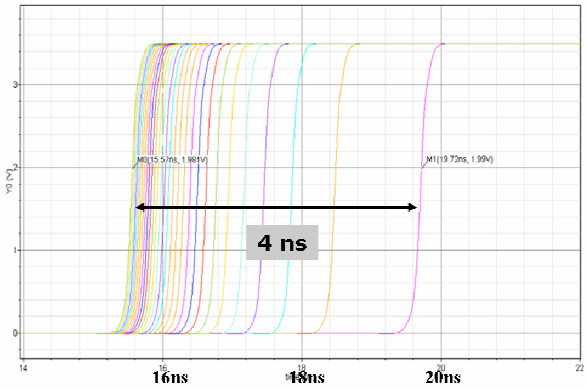


Figure 15: Enlargement of the discriminator rise time.

IV. Conclusion

PARISROC is a dedicated circuit to readout the photomultiplier array. It was designed in AMS SiGe 0.35µm and sent in fabrication in June 2008. The circuits are expected for end of September. The test board is now in layout and will be available in end of October. The first measurement results will arrive at the end of the year.

V. References

[1] B. Genolini et Al., PMm2: large photomultipliers and innovative electronics for next generation neutrino experiments, NDIP'08 conference.

[2] http://pmm2.in2p3.fr/

[3] F. Dulucq et Al., Digital part of PARISROC: a photomultiplier array readout chip, TWEPP08 conference.

[4] http://asic.austriamicrosystems.com/